System overview

Features

User Interface

Measurement Examples

# Integrated Gigasample Processor

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Dimtel, Inc., Redwood City, CA, USA

July 11, 2007



System overview	Features	User Interface	Measurement Examples	Summary
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- Introduction
- Operating experience
- 2 Features
  - Specification highlights
  - Architecture
  - Important features
  - Front and Back End
- 3 User Interface
  - Controls
  - Diagnostics



Measurement Examples

- Photon Factory
- DAΦNE



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iGp Highlig	hts			







- A 500+ MHz processing channel.
- Finite Impulse Response (FIR) bunch-by-bunch filtering for feedback.
- Control and diagnostics via EPICS soft IOC on Linux.
- External triggers, fiducial synchronization, low-speed ADCs/DACs, general-purpose digital I/O.

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- DAΦNE: two systems, transverse feedback;
- Photon Factory (KEK): one system, longitudinal feedback.

- Gproto tests:
  - PEP-II transverse feedback;
  - KEKB transverse feedback;
  - ATF damping ring longitudinal feedback;
  - DAΦNE transverse feedback;
  - PEP-II bunch-by-bunch luminosity monitor.

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Features o●○○○○○○ User Interface

Measurement Examples

# iGp Specifications

# Design goals:

- Reliability;
- Maintainability;
- Ease of use;
- Diagnostics.
- FPGA based processing:
  - Flexible;
  - Field upgradable.

#### Specifications

Bunch spacing  $\geq$  1.9 ns

Harmonic number 64–5120

ADC resolution 8 bits

DAC resolution 12 bits

Feedback filter 16-tap FIR

Downsampling 1-32

DAQ memory 8 MB

Digital GPIO 32 channels

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Slow analog I/O 8 channels



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#### Architecture

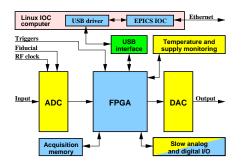
- Important features
   Event and Reals Fig.
- Front and Back End

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# System Block Diagram



- Real-time processing in the FPGA.
- Low-rate (≤ 10 Hz) diagnostics via USB.
- 8 MB memory:
  - Data acquisition in normal operation;
  - Can be used for grow/damps, other diagnostics;
  - Internal or external data acquisition triggers.

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Important F	eatures			

- ADC and DAC timing adjustment with 10 ps step size.
  - Eliminates the need for mechanical delay lines.
- High bandwidth
  - 1.26 GHz input bandwidth;
  - 212 and 328 ps output rise and fall times.
- Self-test program for verifying system health.
  - Generated report can be compared to factory results using "diff".
- User-friendly IOC setup program
  - With a series of windows leads the user through network setup, date/time setting, and IOC name.

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Front/Back-	end Unit			

#### • Currently under development.

- 2U 19" rackmount chassis, just like the iGp.
- 1.4 GHz front-end detection frequency.
- Combiner-based 4-cycle comb generator.
- 892 MHz back-end frequency.
- Integrated control via iGp GPIO:
  - Front and back-end LO phase shifters;
  - Front and back-end attenuators.
- Can be adapted for the ALS:
  - 1.5 GHz detection;
  - 1 GHz output.



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Top-Level F	Panel			

SYSTEM: IGPF	DEVICE: TEST	HELP EXIT
	FEEDBACK ON	
	다 setup	

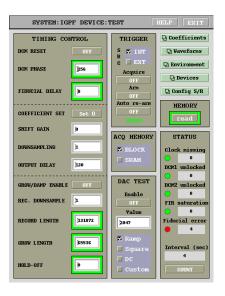
- Top-level panel is kept very simple on purpose.
- One control: feedback on/off.
- Error summary:
  - Green no errors;
  - Yellow warning (saturation);

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• Red - error.

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# **Control Panel**



#### Controls:

- Timing;
- Feedback;
- Data acquisition;

#### • Status:

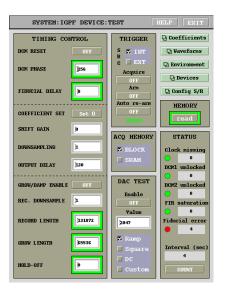
- RF clock;
- FPGA DCMs (digital clock managers);

- Saturation;
- Fiducial.



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# **Control Panel**



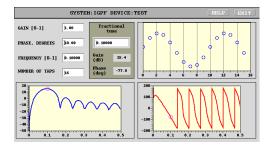
- Controls:
  - Timing;
  - Feedback;
  - Data acquisition;
- Status:
  - RF clock;
  - FPGA DCMs (digital clock managers);

- Saturation;
- Fiducial.



System overview	Features 00000000	User Interface	Measurement Examples	Summary





- Integrated filter generator and analyzer.
- Computes frequency response.
- Gain and phase readout at the tune frequency.
- Filter tuning made easy.

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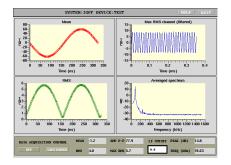
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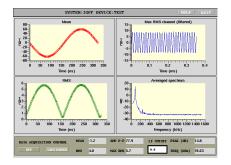
- From bunch data matrix to vectors:
  - Bunch-by-bunch mean and RMS;
  - Time record of the most unstable bunch;
  - Averaged spectrum.
- From vectors to scalars for stripcharting:
  - Mean;
  - Overall and maximum RMS;
  - Peak-to-peak amplitude;
  - Spectral peak frequency and magnitude.

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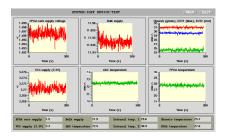
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System H	ealth			



- Built-in monitoring of supply voltages and system temperatures.
- Voltages:
  - FPGA core;
  - Global 3.3 V;
  - Bulk supply (12 V).
- Temperatures:
  - ADC;
  - FPGA;
  - Board temperature;

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• ECL clock delays.



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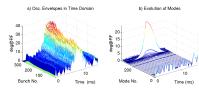
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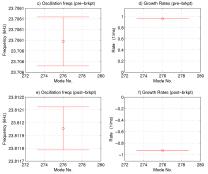


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#### Photon Factory Longitudinal Grow/Damp





PF:jun3007/215154: lo= 200mA, Dsamp= 1, ShifGain= 0, Nbun= 312, At Fs: G1= 0.10338, G2= 0.1723, Ph1= 65.515, Ph2= 65.5215, Brkpt= 20000, Calib= 1.

- A test as a longitudinal feedback.
- 500.1 MHz RF, 312 bunches.
- Growth and damping rates of 1 ms<sup>-1</sup>.

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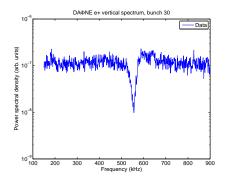
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# DAΦNE Steady-state Recording



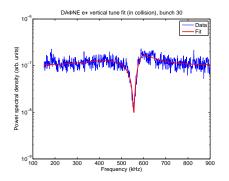
- Vertical feedback in the positron ring.
- 368 MHz, 120 bunches.
- Bunch spectrum shows a notch due to feedback action.
- Fit the spectrum using the feedback/beam model.
- Extract bunch-by-bunch tunes.

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• Completely parasitic!



### DAΦNE Steady-state Recording



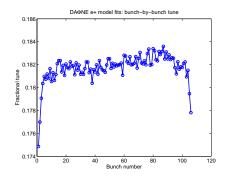
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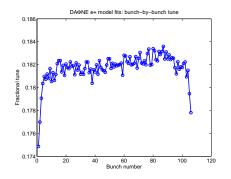
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- iGp is a proven bunch-by-bunch feedback and diagnostic platform.
- Integrated tools make for extremely simple system configuration and maintenance.
- Powerful diagnostics provide real-time stability and performance tracking.
- Direct interface to sophisticated Matlab analysis tools for machine studies.



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