Dimtel Digital Low-level RF LLRF9 For SPEAR3

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Dimtel, Inc., San Jose, CA, USA

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Overview LLRF9 Introduction Inputs and Interlock Feedback Loops Diagnostics

Proposed Architecture Overall Topology Issues Needing Clarification

LLRF Characterization Frequency Domain Time Domain

Stability Measurements and Precision Calibration Thermal Tuning Scans Beam-Based Calibration

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A single 2U chassis;

- 9 input RF channels;
- 2 output RF channels:
 - Amplified;
 - ► Filtered;
 - Interlocked.
- Two spare outputs.

- Tuner motor control;
- External interlock daisy-chain;
- Two external trigger inputs;
- Eight opto-isolated baseband ADC channels.

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Installations and Demos

Machines

Ring	Stations	Cavities
ELSA	1	2
KARA	2	4
KARA booster	1	1
SESAME	4	4
SESAME booster	1	1
DELTA	2	2
Diamond booster (demo)	1	1
LNLS (demo)	2	2
LNLS booster (demo)	1	1



- System is in daily operation at 4 storage rings and 2 boosters;
- Successfully demonstrated at 3 other rings;
- Power sources klystrons, SSAs, IOTs.

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- Each of 9 input channels is monitored at 10 SPS;
- Phase measurements are relative to the master oscillator phase reference at the front panel;
- All RF components are mounted on a 10 mm cold plate with active temperature stabilization;
- Each channel can be configured for voltage or power measurements;
- Hardware phase offsets and full scale levels calibrated for rapid chassis swap;
- Precision calibration procedures for voltage and power.

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Interlock Chain

ID=LLRF: BRD1 HELP EXIT				
INTERLOCKS				
EXTERNAL INTER	LOCK INPUT	ENABL E		MASK
AMPLITUDE	340.74 kv	305.41 kv	625.42 kW	
THRESHOLD	380.00 kv	340.00 kv]780.00 kw	
RAW AMPLITUDE	6364.5 counts	5952.9 counts	6207.6 counts	6098.0 counts
RAW THRESHOLD	7098	6627	6932	8191
EXTERNAL	CHANNEL O	CHANNEL 1	CHANNEL 2	CHANNEL 3
RESET	RESET	RESET	RESET	RESET
5782454	36046144	36067981	92105109	
TRIP CAPTURE	7122	6671	6957	
TRIP VALUE	381.30 kv	342.26 kV	785.54 kw	

Fast interlock threshold can be set for each of 9 RF inputs;

- Guaranteed trip in 11 ADC clock cycles (100 ns);
- Multiple layers of interlock protection for drive outputs. On interlock trip:
 - Hardware controlled RF switch is opened;
 - FPGA DAC drive is set to zero;
 - DAC is disabled (hardware powerdown);
 - DDR output flip-flop is held reset.

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Interlock Output Path



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LLRF	HELP
INTERLOCK STATUS	RESET
TRIP SOURCE	TIME
CAVITY 1 PROBE1	0.000 us
CAVITY 2 PROBE1	384.022 us
Board 1 interlock Board 2 interlock	Board 3 interlock

- External interlock enable input and interlock output allow for easy daisy-chaining:
 - Opto-isolated input;
 - 5 volt logic and solid-state relay output.
- Spare output used in some machines as HVPS enable/interlock;
- All interlock sources are timestamped;
- IOC automatically sorts events to simplify trip diagnostics.

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- Single cavity or vector sum of two;
- Reference phase is compensated in real-time;
- Proportional (direct) and integral loops;

- Double rate DAC drive;
- 512-point amplitude and phase profiles;
- Excitation input for built-in network analyzer.

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Tuner Loop



Loop runs in the EPICS IOC at 10 Hz;

- Keeps cavity forward and probe phases aligned;
- Options for one or two motors per cavity, field balancing loop for multi-cell cavities;
- Adjustable deadband to avoid unnecessary mechanical wear.

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ID=LLE1:C1T1	HELP EXIT	
GALIL DMC-21X3 STREAM DEVICE		
VELOCITY COMMAND)0.000 deg/s	
ENCODER POSITION	315691.920 deg	
ENCODER VELOCITY	0.000 deg/s	
ANALOG INPUT	-5.549 V	
MOVING ENABLE I	DIR COWLIM OWLIM	
•	см 😑 😑	
DISABLE ENABLE	STATUS 0x6D	

LLRF9 supports a number of off-the-shelf motor controllers:

- Galil DMC-21X3 stepper/brushed DC/brushless;
- Schneider Electric Motion Mdrive Plus stepper;
- Aerotech Soloist brushed DC.
- Interfaces include Ethernet, RS-485, RS-422;
- Plunger position monitoring from analog potentiometer;
- Standard support for limit switches;
- EPICS MotorRecord is supported, not recommended.

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ID=LLRF: C1T1 HELP EXIT	
MOTOR RECORD	
POSITION (DEG)	<u>]-6607.06</u>
RELATIVE VALUE (DEG)	0.00
VELOCITY (DEG/S)	5000.00
ACCELERATION TIME (S)	<u>)</u> 0.040
DIRECTION OF TRAVEL	0
RAW MOTOR POSITION	-939567
READBACK VALUE (DEG)	-6606.33047
ANALOG INPUT	986
DONE MOVING LOW LIM HI LIM	

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Top Level Panel: ANKA



Two cavity station (ANKA):

- ► 6 cavity signals;
- Klystron forward and reflected;
- Magic T load.

- Two tuner loops;
- Active blocks for quick control panel access.

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 - Magic T load.

Two tuner loops;

 Active blocks for quick control panel access. Overview LLRF9 Introduction Inputs and Interlock Feedback Loops Diagnostics

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Top Level Panel: ANKA



- Two cavity station (ANKA):
 - ► 6 cavity signals;
 - Klystron forward and reflected;
 - Magic T load.

- Two tuner loops;
- Active blocks for quick control panel access.

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Top Level Panel: SESAME



- Two single cavity stations (SESAME):
 - 3 cavity signals per station;
 - BPM sum;
 - 2 spare signals.

- Two tuner loops;
- Station state machine controls.

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Top Level Panel: SESAME



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Top Level Panel: SESAME



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- Two single cavity stations (SESAME):
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- Station state machine controls.

State Machine



Simplified controls: ON and OFF;

- State machine handles station turn on
 - Cavity tuning in open loop state;
 - Feedback loop closure;
 - Ramping to nominal field;
 - Rampdown and turn-off.
- Monitors error conditions (interlocks) and timeouts.

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- 12 ADC channels sampling IF signals (9 inputs, 3 references);
- 24576 sample buffer;
- 10 updates per second in free running mode;
- Multiple hardware trigger sources:
 - External trigger;
 - Ramp profile start;
 - Interlock;
 - Feedback loop closure.
- Supports pre-trigger acquisition for trip capture.

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ID=LLRF: BRD1 HELP EXIT	
ACQUISITION CONTROLS	
POST-TRIGGER LENGTH]16384
CH2/CH3 WAVEFORM	ADC2/ADC3
TRIGGER SELECT	SOFTWARE
	HARDWARE
HARDWARE TRIGGER	

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- High resolution (1024 point) swept analyzer;
- Adjustable excitation level;
- Fast sweep times with proprietary carrier suppression algorithm;
- Multiple probe points within the system:
 - Cavity probe;
 - Cavity sum;
 - Error signal;
 - Drive output.
- Spectrum analyzer mode with excitation disabled.

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- 3 LLRF4.6 modules, each with 4 RF inputs;
- One input per module dedicated to reference monitoring;
- Identical FPGA code on all 3 modules;
- Two complete field control paths with filtering/interlocking.

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Proposed Topology



- Need 12 channels to monitor 4 cavities (probe, forward, reflected) — at least two units;
- PEP-II setup monitors 23 channels plus reference;
- Delete 5 channels or add a third unit?
- Top unit monitors all probe and forward signals:
 - Field control loops;
 - Four tuner loops are on that IOC as well.
- Bottom LLRF9/476 is monitoring/interlock only.

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- Initial plan use two cavity vector sum (OUT0);
- Plus four tuner loops;
- To measure the transfer functions through cavities 3 and 4 need to add OUT2 to OUT0;
- Realized that two field control loops can run in parallel;
 - Closer to a 4 cavity vector sum;
 - Care needed in configuration (more on next slide).

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- Integral loops zero Δ at RF;
- Two integrators on at once balancing problems;
- Direct loop with moderate gain is more tolerant;

Two direct, one integral;

- Integral: high gain at low frequencies;
- Direct: 12–15 dB of wideband feedback for all 4 cavities.

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Total number of channels and channel selection;

- Tuner motor control;
- HVPS control/interlocking;
- Opto-isolated slow ADC and interlocking;
 - Each LLRF9 includes an 8 channel 12 bit opto-isolated ADC;
 - Capable of triggering interlocks (window comparator);
 - Four configurable input ranges: $\pm 5 \text{ V}, \pm 10 \text{ V}, 0-5 \text{ V}, 0-10 \text{ V};$
 - Each channel is polled at 13.75 ksps.
- Interlock daisychain input and output;
- Digital input levels, connectors.

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Development needed

Configure 4 tuner loops (easy);

- Structure to integrate monitoring information from multiple LLRF9 units;
- Top-level interlock summary processor, reset handler;
- Operating procedure for dual loop operation
- State machine to run SPEAR3 configuration.

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- Measured from setpoint to the cavity probe;
- Feedback block in open loop has no dynamics, just gain and phase shift;
- Open loop cavity response;
- ► Fit resonator model to extract gain, loaded *Q*,
- Extremely useful for configuring the feedback loops, tuner loops, general diagnostics.

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- Measured from setpoint to the error signal;
- Shows attenuation at frequencies where feedback has gain;
- Perturbations at the input of the cavity are rejected with the same transfer function;
- Proportional only;
- Proportional and integral, much higher rejection at low frequencies;
- Easier to see with the logarithmic frequency scale.

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- Perturbations at the input of the cavity are rejected with the same transfer function;
- Proportional only;
- Proportional and integral, much higher rejection at low frequencies;
- Easier to see with the logarithmic frequency scale.

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Ramp start triggers waveform acquisition;

- Ramp profile loaded with a 10% amplitude step (230 to 253 kV);
- Open loop: phase shift (AM-PM in power stage), setpoint error;
- Closed loop response is much faster, as expected;
- A bit too much gain, overshoot seen;
- Prominent ripple due to SSA power supply switching at 190 kHz.

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Open-loop pulse response, cavity A;

- Base 2 kV, pulse 20 kV;
- Larger reflected power peak at the falling edge, expected for coupling factor β > 1;
- Phase slope during pulse decay indicates the cavity is slightly detuned

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9 internal sensors on cold plate: 6 NTCs, 3 DS18B20 digital sensors;

- Three temperature stabilization loops using thermoelectric coolers;
- Two external sensors, in air and attached to chassis;
- Tight stabilization of in-loop sensors;
- Residual sensitivity of out-of-loop sensors is 0.09–0.12 °C/°C.

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Recorded over 2 days;

- Diurnal temperature variation clearly seen in out of loop sensors and Peltier control signals;
- Out of loop NTC sensors show 0.22 °C peak-to-peak variation

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Tuning Scan at SESAME

- Run the station in open loop, fixed setpoint;
- Move the cavity from limit switch to limit switch;
- At multiple points record:
 - Probe voltage and phase;
 - Forward and reflected power and phase;
 - LLRF9 output power meter;
 - Tuner potentiometer;
 - Open-loop transfer function.
- A lot of interesting plots!

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Tuner Position Potentiometer vs. Detuning



- Nearly linear;
- A deviation near zero detuning is caused by wall heating;
- Slope should be consistent, offset shifts with temperature.

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Cavity Voltage vs. Detuning



Cavity voltage peaks around 0;

- Zooming in we see an interesting effect — peak voltage is around 650 Hz;
- Likely due to imperfect match at the SSA output.

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- Reflected power minimum near 0;
- Forward power reading changes due to finite directivity of couplers;
- Drive level is constant;
- Peak field and minimum reflected are offset;
- Offset minimum of reflected power is expected, directivity again.

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- Assuming power source is matched, we compute the coupler directivity correction matrix;
- At each point, we compute the expected reflection coefficient at RF from cavity transfer function fit;
- Matrix elements are then adjusted to:
 - Remove variation in forward power;
 - Match measured and computed reflection.

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Time Domain Cavity Response



Step drive to 0;

- Natural cavity response;
- Can extract quality factor and detuning;
- At the same tuning point collected 20 transfer function measurements;
- Roughly 300 Hz offset between frequency and time domain.

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Cavity Parameters at LNLS



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Probe Calibration



 Scanned cavity 1 field down to 170 kV, captured synchrotron tune using LFB tune tracking;

Fit ω_s to total voltage V_g assuming:

- Stations are in phase (phased earlier to maximize ω_s);
- Momentum compaction, beam energy, energy loss per turn are as published.
- Obtain scaling factors for existing calibrations.

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- LLRF9 integrates a lot of functionality in a single unit;
- Used with normal conducting cavities at a number of machines
- Powerful diagnostic features to simplify tuning and operation;
- Enables precision measurements of accelerator parameters

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