

Integrated Gigasample Processor

Dmitry Teytelman

Dimtel, Inc., Redwood City, CA, USA

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Outline

- 1 System overview
 - Introduction
 - Operating experience
- 2 Features
 - Specification highlights
 - Architecture
 - Important features
 - Front and Back End
- 3 User Interface
 - Controls
 - Diagnostics
- 4 Measurement Examples
 - Photon Factory
 - DAΦNE

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iGp Highlights



- A 500+ MHz processing channel.
- Finite Impulse Response (FIR) bunch-by-bunch filtering for feedback.
- Control and diagnostics via EPICS soft IOC on Linux.
- External triggers, fiducial synchronization, low-speed ADCs/DACs, general-purpose digital I/O.

What's Inside



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Installed Units and Tests

- iGp is installed or has been tested in the following machines:
 - DAΦNE: two systems, transverse feedback;
 - Photon Factory (KEK): one system, longitudinal feedback.
- Gproto tests:
 - PEP-II transverse feedback;
 - KEKB transverse feedback;
 - ATF damping ring longitudinal feedback;
 - DAΦNE transverse feedback;
 - PEP-II bunch-by-bunch luminosity monitor.

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iGp Specifications

- Design goals:
 - Reliability;
 - Maintainability;
 - Ease of use;
 - Diagnostics.
- FPGA based processing:
 - Flexible;
 - Field upgradable.

Specifications

Bunch spacing ≥ 1.9 ns

Harmonic number 64–5120

ADC resolution 8 bits

DAC resolution 12 bits

Feedback filter 16-tap FIR

Downsampling 1-32

DAQ memory 8 MB

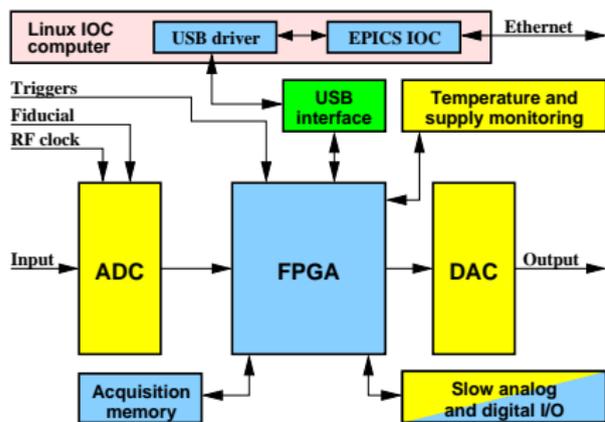
Digital GPIO 32 channels

Slow analog I/O 8 channels

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System Block Diagram



- Real-time processing in the FPGA.
- Low-rate (≤ 10 Hz) diagnostics via USB.
- 8 MB memory:
 - Data acquisition in normal operation;
 - Can be used for grow/damps, other diagnostics;
 - Internal or external data acquisition triggers.

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Important Features

- ADC and DAC timing adjustment with 10 ps step size.
 - Eliminates the need for mechanical delay lines.
- High bandwidth
 - 1.26 GHz input bandwidth;
 - 212 and 328 ps output rise and fall times.
- Self-test program for verifying system health.
 - Generated report can be compared to factory results using "diff".
- User-friendly IOC setup program
 - With a series of windows leads the user through network setup, date/time setting, and IOC name.
- DAC test pattern generator.

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Front/Back-end Unit

- **Currently under development.**
- 2U 19" rackmount chassis, just like the iGp.
- 1.4 GHz front-end detection frequency.
- Combiner-based 4-cycle comb generator.
- 892 MHz back-end frequency.
- Integrated control via iGp GPIO:
 - Front and back-end LO phase shifters;
 - Front and back-end attenuators.
- Can be adapted for the ALS:
 - 1.5 GHz detection;
 - 1 GHz output.

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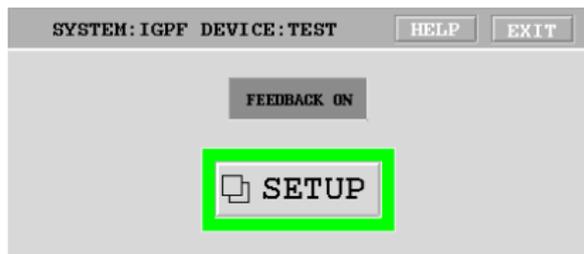
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Top-Level Panel



- Top-level panel is kept very simple on purpose.
- One control: feedback on/off.
- Error summary:
 - Green - no errors;
 - Yellow - warning (saturation);
 - Red - error.

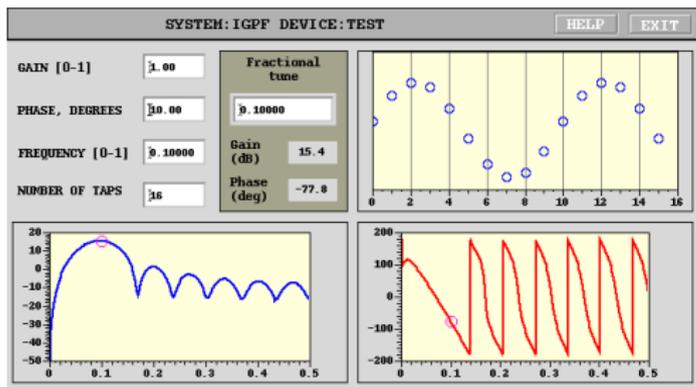
Control Panel

SYSTEM: IGPf DEVICE: TEST HELP EXIT

TIMING CONTROL	TRIGGER	<input type="checkbox"/> Coefficients
DCM RESET OFF	S <input checked="" type="checkbox"/> INT	<input type="checkbox"/> Waveforms
DCM PHASE 256	R <input type="checkbox"/> EXT	<input type="checkbox"/> Environment
FIDUCIAL DELAY 0	Acquire	<input type="checkbox"/> Devices
	OFF	<input type="checkbox"/> Config S/R
COEFFICIENT SET Set 0	Arm	
SHIFT GAIN 0	OFF	MEMORY
DCM SAMPLING 1	Auto re-arm	<input type="checkbox"/> read
OUTPUT DELAY 120	OFF	
	RESET	
GROW/DAMP ENABLE OFF	ACQ MEMORY	STATUS
REC. DOWNSAMPLE 1	<input checked="" type="checkbox"/> BLOCK	Clock missing
RECORD LENGTH 131072	<input type="checkbox"/> SRAM	<input type="checkbox"/> 0
GROW LENGTH 85536	DAC TEST	DCM1 unlocked
HOLD-OFF 0	Enable	<input type="checkbox"/> 0
	OFF	DCM2 unlocked
	Value	<input type="checkbox"/> 0
	2047	FIR saturation
	<input checked="" type="checkbox"/> Ramp	<input type="checkbox"/> 0
	<input type="checkbox"/> Square	Fiducial error
	<input type="checkbox"/> DC	<input type="checkbox"/> 4
	<input type="checkbox"/> Custom	Interval (sec)
		<input type="checkbox"/> 4
		COUNT

- Controls:
 - Timing;
 - Feedback;
 - Data acquisition;
- Status:
 - RF clock;
 - FPGA DCMs (digital clock managers);
 - Saturation;
 - Fiducial.

Coefficient Generator

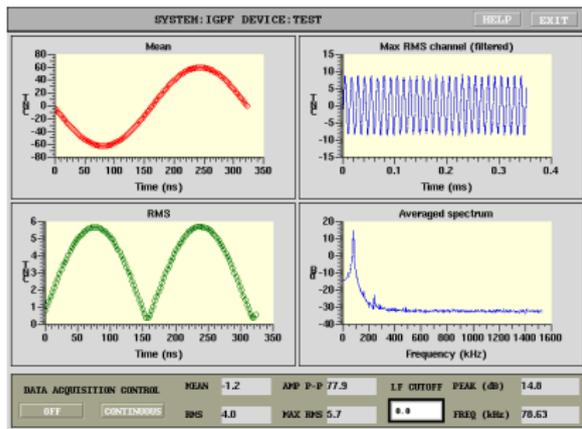


- Integrated filter generator and analyzer.
- Computes frequency response.
- Gain and phase readout at the tune frequency.
- Filter tuning made easy.

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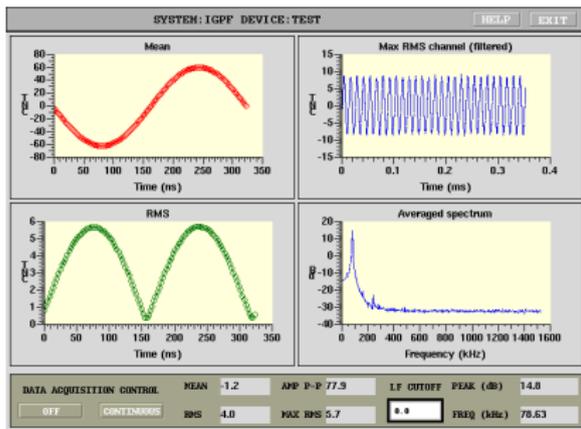
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Waveform Display



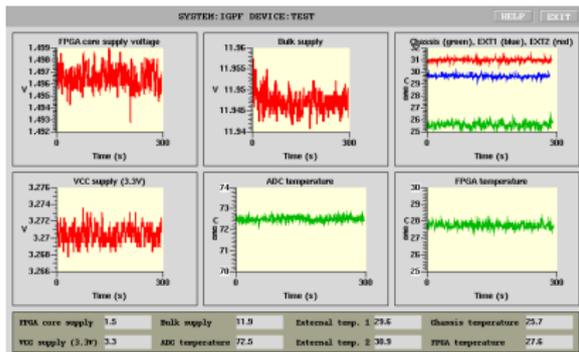
- From bunch data matrix to vectors:
 - Bunch-by-bunch mean and RMS;
 - Time record of the most unstable bunch;
 - Averaged spectrum.
- From vectors to scalars for stripcharting:
 - Mean;
 - Overall and maximum RMS;
 - Peak-to-peak amplitude;
 - Spectral peak frequency and magnitude.

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System Health



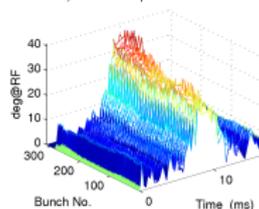
- Built-in monitoring of supply voltages and system temperatures.
- Voltages:
 - FPGA core;
 - Global 3.3 V;
 - Bulk supply (12 V).
- Temperatures:
 - ADC;
 - FPGA;
 - Board temperature;
 - ECL clock delays.

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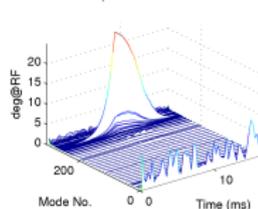
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Photon Factory Longitudinal Grow/Damp

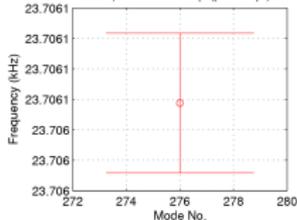
a) Osc. Envelopes in Time Domain



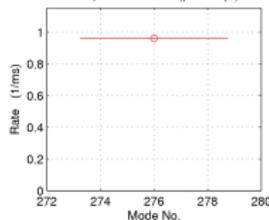
b) Evolution of Modes



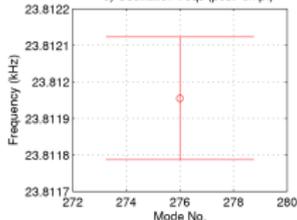
c) Oscillation freqs (pre-brkpt)



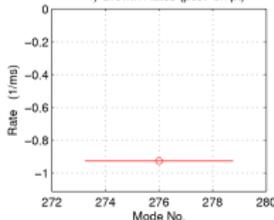
d) Growth Rates (pre-brkpt)



e) Oscillation freqs (post-brkpt)



f) Growth Rates (post-brkpt)

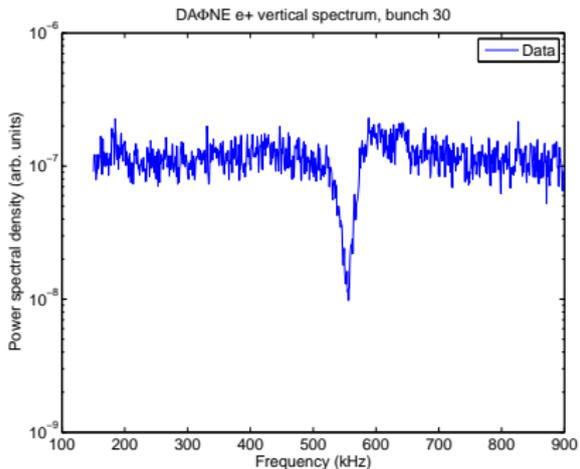


- A test as a longitudinal feedback.
- 500.1 MHz RF, 312 bunches.
- Growth and damping rates of 1 ms^{-1} .

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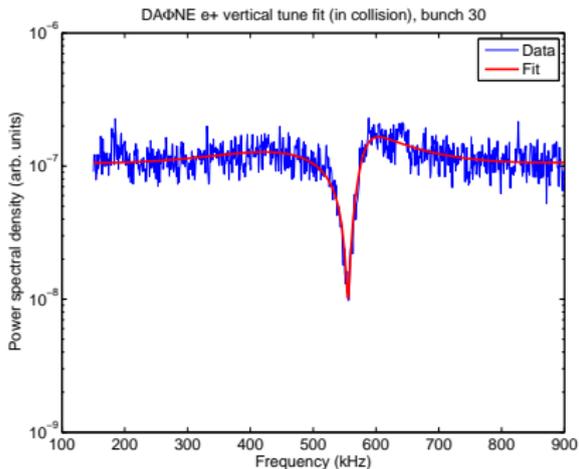
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DAΦNE Steady-state Recording



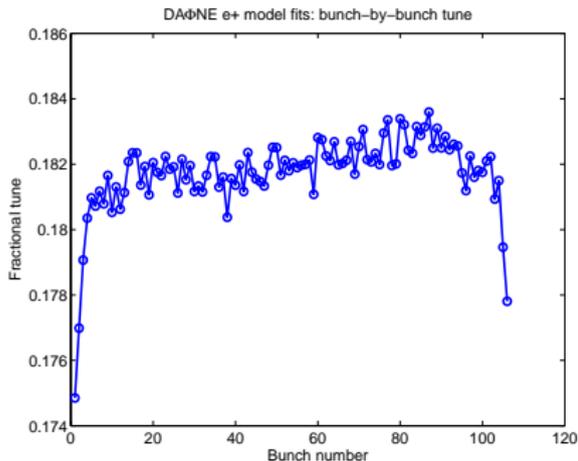
- Vertical feedback in the positron ring.
- 368 MHz, 120 bunches.
- Bunch spectrum shows a notch due to feedback action.
- Fit the spectrum using the feedback/beam model.
- Extract bunch-by-bunch tunes.
- **Completely parasitic!**

DAΦNE Steady-state Recording



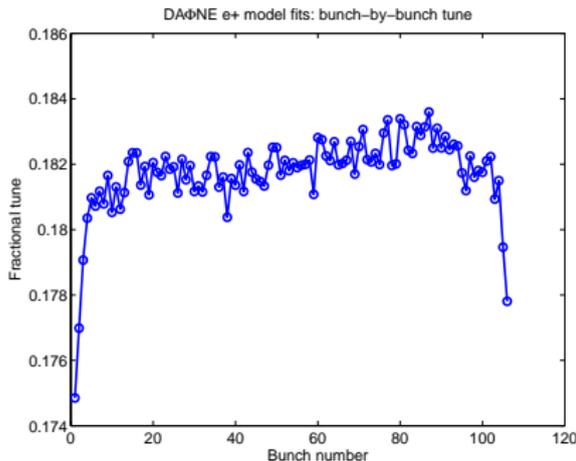
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- iGp is a proven bunch-by-bunch feedback and diagnostic platform.
- Integrated tools make for extremely simple system configuration and maintenance.
- Powerful diagnostics provide real-time stability and performance tracking.
- Direct interface to sophisticated Matlab analysis tools for machine studies.

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