

LLRF SYSTEM FOR THE FERMILAB MUON G-2 AND MU2E PROJECTS^{*†}

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Abstract

The Mu2e experiment measures the conversion rate of muons into electrons and the Muon g-2 experiment measures the muon magnetic moment. Both experiments require 53 MHz batches of 8 GeV protons to be re-bunched into 150 ns, 2.5 MHz pulses for extraction to the g-2 target for Muon g-2 and to a delivery ring with a single RF cavity running at 2.36 MHz for Mu2e. The LLRF system for both experiments is implemented in a SOC FPGA board integrated into the existing 53 MHz LLRF system in a VXI crate. The tight timing requirements, the large frequency difference and the non-harmonic relationship between the two RF systems provide unique challenges to the LLRF system design to achieve the required phase alignment specifications for beam formation, transfers and beam extinction between pulses. The new LLRF system design for both projects is described and the results of the initial beam commissioning tests for the Muon g-2 experiment are presented.

INTRODUCTION

The Muon $g-2$ experiment at Fermilab will measure the muon anomalous magnetic moment, $a_\mu = (g-2)/2$, to a precision of 0.14 parts per million (ppm). Mu2e proposes to measure the ratio of the rate of the neutrinoless, coherent conversion of muons into electrons in the field of a nucleus, relative to the rate of ordinary muon capture on the nucleus. The muon beam is created by an 8 GeV proton beam striking a production target and a system of superconducting solenoids that efficiently collect pions and transport their daughter muons to a stopping target [1, 2]. The location of the various RF components and the accelerator systems are shown in Fig. 1.

The existing LLRF system for Recycler supports slip-stacking and transfers of 53 MHz beam from the Booster and to the Main Injector respectively. For the $g-2$ and the Mu2e experiments, a 53 MHz batch from the Booster is re-bunched into 2.5 MHz bunches by adiabatic ramping and transferred to the $g-2$ target or to the Delivery Ring (DR) for the Mu2e project. Seven 2.5 MHz cavities in the Recycler provide the RF voltage for the adiabatic ramping. A single 2.36 MHz cavity is used in the Delivery Ring to capture the beam transferred from the Recycler. The

new LLRF system provides the RF drives to these cavities and supports the adiabatic ramping and transfer control of the rebunched beam to the $g-2$ target and the Delivery Ring. The new LLRF system is implemented on a VXI FPGA board using a Cyclone V SOC FPGA which integrates an FPGA and a high performance floating point dual core ARM microprocessor on the same chip.

LLRF SYSTEM

The new LLRF system is integrated into the Recycler LLRF system VXI crate. The location of the 53 MHz, 2.5 MHz and 2.36 MHz RF drives in the same crate under the control of one slot0 controller provides a common machine control interface and the capability to execute the beam manipulations and transfers between machines. The RF frequency of 2.36 MHz of the Delivery Ring is not harmonically related to the Recycler 2.5 MHz. This makes it challenging to transfer beam with phase alignment between the machines. The FPGA I/O is 3.3V or lower and the existing LLRF system signals are 5V TTL. A signal conditioning analog I/O board also in a VXI form factor is placed in an adjacent slot in the VXI crate to take advantage of the backplane local bus connections. This signal conditioning module also provides the filtering and amplification of the RF drives and the comparators for generating RF clocks.

The 2.5 MHz RF is generated by a digital PLL locked to the 53 MHz. The 2.36 MHz RF is generated by a NCO which has controls for phase resets and offsets which is useful for the phase alignment during beam transfers. Extraction synch pulses for beam transfers and marker signals to indicate the bucket location of the beam are also generated in the FPGA logic. The FPGA board has sixteen 14

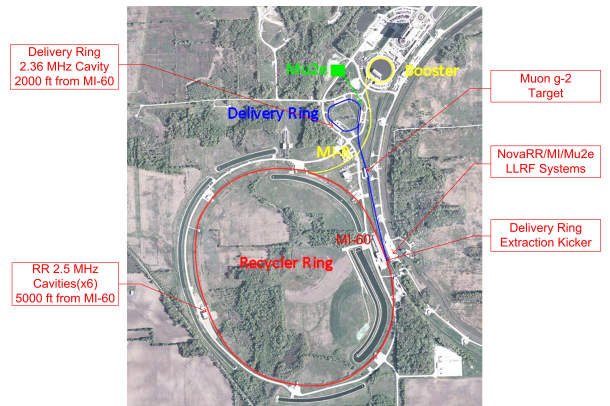


Figure 1: RF system components

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[†] Work supported by Fermi Research Alliance LLC. Under DE-AC02-07CH11359 with U.S. DOE.

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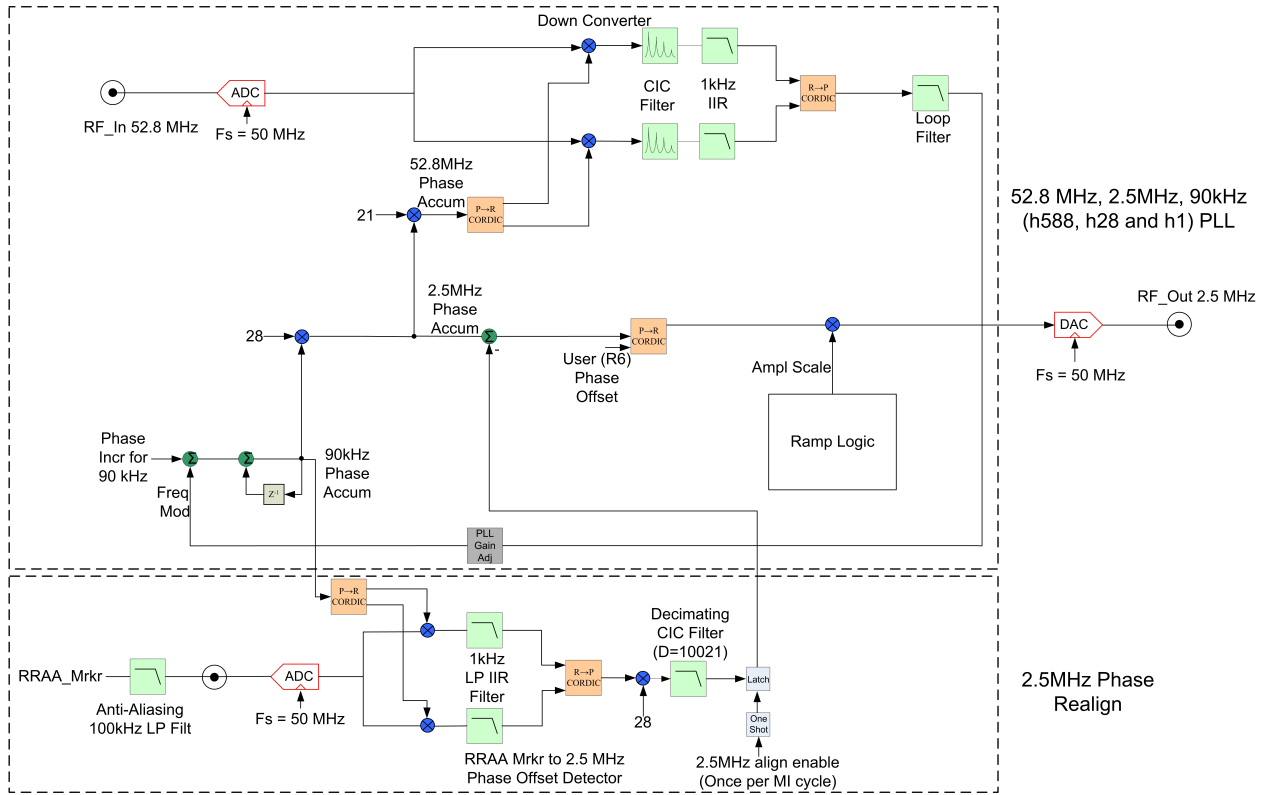


Figure 2: Digital PLL with Phase Alignment

bit ADC channels with a max sample rate of 65 MSPS and eight 14 bit DAC channels with a max sample rate of 260 MSPS. A stable 50 MHz external clock source is used by the existing Recycler LLRF system which is also used in the new board. Cavity signals such as RF voltage sum and accelerator signals such as BPMs and wall current monitor are digitized and processed to measure parameters such as cavity voltage, radial position and beam phase.

DIGITAL PLL ARCHITECTURE

The 53 MHz LLRF systems for the Main Injector and the Recycler both use a common 50 MHz high stability clock reference. Using this frequency as the system clock in the FPGA board is a reasonable and practical choice for this application. The 53 MHz RF reference can be sampled at the 50 MHz clock rate providing the digital reference signal for the PLL. Since a division in the fixed point arithmetic of the FPGA is both resource heavy and time consuming, a PLL architecture based on multipliers is used in this design. In addition to the 2.5 MHz, a 90kHz signal ($h=1$), that is critical for the phase alignment of the 2.5 MHz, can also be generated easily as part of this design. The digital PLL architecture is shown in Fig. 2.

The phase accumulator and CORDIC block (polar to rectangular) together act like the NCO providing the quadrature signals for the downconverter. The downconverter with a rectangular to polar CORDIC forms the phase detector. The phase error signal at the output of the down-

converter needs to be low pass filtered to remove the down-conversion products as shown in fig2. In order to conserve FPGA resources, a combination of a CIC and an IIR filter is used providing an attenuation of 100 dB to the sidebands at ± 5.6 MHz. A non-decimating CIC of order 9 is used which has a zero at $50 \times 1/9 = 5.56$ MHz. The IIR filter is a Chebyshev Type II first order low pass filter. The loop filter is a single zero and single pole filter which allows for a high PLL gain with a phase margin of nearly 90 degrees.

There are three phase accumulators in the PLL loop corresponding to the three frequencies - 90 kHz ($h=1$), 2.5 MHz ($h=28$) and 53 MHz ($h=588$). The filtered phase error is multiplied first by a factor of 28 and then by a factor of 21. The final phase accumulator output is used to generate the 53 MHz to close the PLL loop. All phase accumulators are 30 bits wide for ease of implementation in the FPGA. It must be noted that the two multipliers in the loop contribute a factor of 588 in the loop gain. A simple bit shifting gain adjust block provides gain adjustment in 6 dB steps. The 90 kHz phase increment provides the nominal frequency of the loop to which the loop filter output is added to provide the frequency modulation for the PLL loop.

PHASE ALIGNMENT OF 2.5 MHz RF

The process of beam transfer from the Booster to the Recycler involves the designation of a 52.8 MHz bucket zero which is the location of the first batch transferred. A revolution marker called the RRAA marker which is a narrow

TTL pulse ($\sim 130\text{ns}$) with a frequency $52.8\text{ MHz}/588 = 89.8\text{ kHz}$ is a signal that is used by many accelerator sub-systems to represent the bucket zero location for the 52.8 MHz beam. When the 52.8 MHz beam is rebunched into 2.5 MHz bunches, the bucket zero location for 2.5 MHz coincides with the bucket zero of the 52.8 MHz beam.

During each machine cycle, the bucket zero location can shift randomly between one of 588 positions wrt the 52.8 MHz RF. Since the 2.5 MHz RF is generated as a divide by 21 of the 52.8 MHz RF and is phase locked to it, its phase with respect to bucket zero can shift to one of 21 locations. Thus a process for detecting this phase shift and providing a correcting phase offset to the 2.5 MHz RF is necessary during each machine cycle.

Within the PLL loop, the 89.8 kHz , 2.5 MHz and 52.8 MHz waveforms are all phase aligned. If we can measure the RRAA marker phase wrt the internal 89.8 kHz phase, in each machine cycle and multiply this value by 28, this will represent the phase offset of the 2.5 MHz with respect to bucket zero. Applying this offset to the 2.5 MHz phase accumulator will provide the desired phase alignment. The internal 89.8 kHz phase accumulator output is the input to the CORDIC based NCO which generates the quadrature waveforms for downconversion of the digitized marker signal. The downconversion I and Q outputs are low pass filtered with an IIR and a decimating CIC filter before being passed through another CORDIC based phase detector. The detected phase offset is multiplied by 28 to get the 2.5 MHz phase offset. This output is latched by the phase correction logic. This method was tested to provide a phase jitter that was less than 1 ns (~ 1 degree at 2.5 MHz).

PLL DESIGN

The basic architecture for a digital PLL is shown in Fig. 3. The downconverter and CORDIC block are equivalent to the phase detector of an analog PLL. The NCO is equivalent to the VCO. When the sampling rate of the digital PLL is very high compared to the PLL loop bandwidth, its analysis can be done by analogy to the equivalent analog PLL. The components of the analog PLL are shown in Fig. 4.

The output of the phase detector can be written as

$$u_1(t) = K_1 \sin[\phi_i(t) - \phi_o(t)] \quad (1)$$

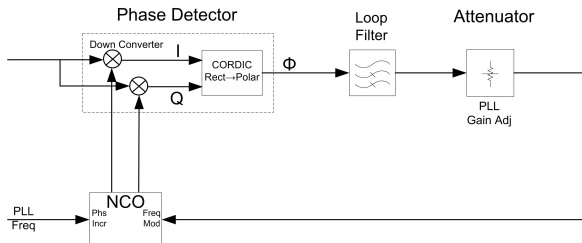


Figure 3: Digital PLL Loop configuration

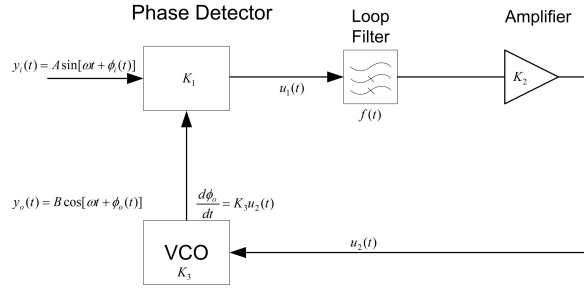


Figure 4: Analog PLL Loop

and

$$u_2(t) = K_2 u_1(t) * f(t) \quad (2)$$

$$\frac{d\phi_o}{dt} = K_3 u_2(t) = K_1 K_2 K_3 \sin[\phi_i(t) - \phi_o(t)] * f(t) \quad (3)$$

When the frequencies are locked and the difference between the input and output phase is small, the following approximation may be applied

$$\frac{d\phi_o}{dt} = K[\phi_i(t) - \phi_o(t)] * f(t) \quad (4)$$

where $K = K_1 K_2 K_3$. Taking the Laplace transform on both sides

$$j\omega \Phi_o(j\omega) = K[\Phi_i(j\omega) - \Phi_o(j\omega)]F(j\omega) \quad (5)$$

the closed loop transfer function may be written as

$$T(j\omega) = \frac{\Phi_o(j\omega)}{\Phi_i(j\omega)} = \frac{KF(j\omega)}{j\omega + KF(j\omega)} \quad (6)$$

From fig 4 the open loop transfer function can be written as

$$G(j\omega) = \frac{KF(j\omega)}{j\omega} = \frac{K}{j\omega(1 + j\frac{\omega}{\omega_1})} \quad (7)$$

where ω_1 is the pole of the first order loop filter. The roots of the closed loop transfer function are found by setting $1 + G(s) = 0$. Writing this in the standard form in terms of the natural frequency ω_n and damping factor ζ as

$$s^2 + 2\zeta\omega_n s + \omega_n^2 = 0 \quad (8)$$

where

$$\omega_n = \sqrt{K\omega_1}, \quad \zeta = \frac{1}{2} \sqrt{\frac{\omega_1}{K}} \quad (9)$$

The poles are located at

$$s = \frac{-\omega_1}{2} \left[1 \pm \sqrt{1 - \frac{4K}{\omega_1}} \right] \quad (10)$$

A single pole loop filter design has the drawback that while we need a low ω_1 to filter out the high frequency ripple from the phase detector, we also need a high loop gain K to reduce the phase error. When the filter pole is less than the crossover frequency, increasing the loop gain reduces the

phase margin. The damping factor is also very small in this case. There is a trade off between the stability of the loop and minimizing the phase error. Adding a zero at ω_2 where $\omega_2 > \omega_1$, provides a solution to this problem by improving the phase margin at high loop gain. The close loop transfer function is now

$$T(s) = \frac{\Phi_o(s)}{\Phi_i(s)} = \frac{(1 + \frac{s}{\omega_2})}{\frac{s^2}{K\omega_1} + s[\frac{1}{K} + \frac{1}{\omega_1}] + 1} \quad (11)$$

with

$$\omega_n = \sqrt{K\omega_1}, \quad \zeta = \frac{1}{2} \sqrt{\frac{\omega_1}{K}} + \frac{1}{2} \frac{\omega_n}{\omega_2} \quad (12)$$

The poles are given by

$$s = -\zeta\omega_n \pm \omega_n\sqrt{\zeta^2 - 1} \quad (13)$$

In order to apply the analysis to the digital PLL the gain factors K_1, K_2, K_3 need to be identified. The phase detector gain K_1 can be obtained from the cordic parameters. The input rectangular co-ordinates are 20 bits and the output phase of $\pm\pi$ is 22 bits. Therefore $K_1 = 2^{21}/\pi$ sec-counts/radian. The seconds in the unit comes from the fact that the downconverter/cordic block can be considered as a frequency to phase conversion block. The frequency modulation input of the NCO is 30 bits and the NCO clock f_s is 50.0 MHz. From the NCO user guide the frequency modulation gain is given by

$$K_3 = \frac{2\pi f_s}{2^{30}} \quad (14)$$

which is in units of radians/sec/count. Assuming a gain adjust of 1 and taking into account the internal multiplier of 588 in the phase loop, $K_2 = 588$ and the maximum PLL loop gain is given by

$$K = K_1 K_2 K_3 = 1.148 \times 10^8 = 161.2 \text{ dB} \quad (15)$$

Since the cordic output is 22 bits, from (14) it is seen that the upper limit for frequency modulation is

$$\frac{2^{21} \times 50.0 \times 10^6}{2^{30}} = \pm 97.66 \text{ kHz} \quad (16)$$

The loop gain adjustment is implemented as a bit shift (right shift only) of the cordic output. This results in the above frequency modulation range being reduced by a factor of 2 and a loop gain reduction by 6 dB per bit shifted (max of 120 dB attenuation).

The PLL parameters to be determined are the loop filter pole and zero ω_1, ω_2 and the gain K . A high gain is desirable to keep the phase error low and a low value for the filter pole will help to reduce the high frequency products from the phase detector. Starting with $K = 10^5 = 100\text{dB}$ and $\omega_1 = 2\pi \times 500$, we can calculate ω_2 to obtain the desired damping factor. Choosing a $\zeta = 2$ to obtain a minimally peaking close loop transfer function and using (12),

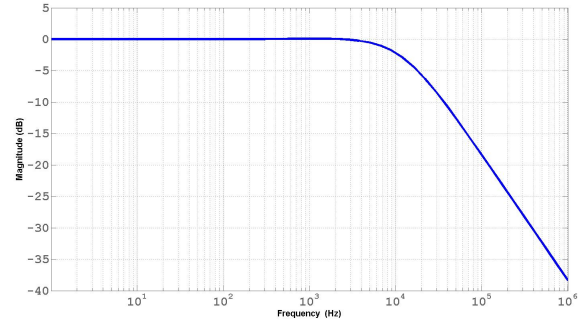


Figure 5: Close Loop Frequency Response

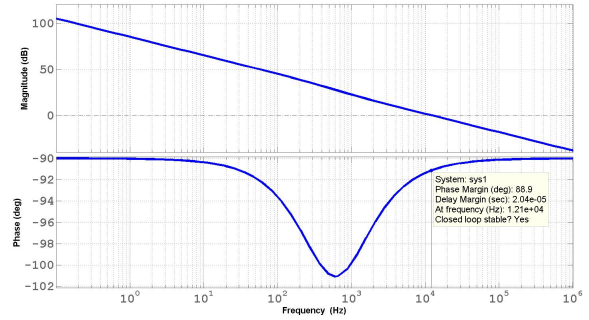


Figure 6: Open Loop Frequency Response

the zero location can be calculated as $\omega_2 = 2\pi \times 738$. Thus the loop filter transfer function is

$$F(s) = \frac{1 + \frac{s}{\omega_2}}{1 + \frac{s}{\omega_1}} \quad (17)$$

The corresponding transfer function in the z-domain is obtained as

$$F(z) = \frac{1 + e^{-\omega_2 T_s} z^{-1}}{1 + e^{-\omega_1 T_s} z^{-1}} \quad (18)$$

To reduce the loop gain to 100 dB, an attenuation of 10 bits is needed in the gain adjust block. The magnitude response of the close loop transfer function is shown in Fig. 5. The bode plot of the open loop transfer function in Fig. 6 shows that the phase margin is 88.9 degrees.

BEAM TRANSFER TO DELIVERY RING

Due to the non-harmonic relationship between the Recycler 2.5 MHz and the DR 2.36 MHz RF frequencies, a specific phase alignment scheme needs to be used for every pulse, to guarantee the transfer of the beam to the DR into the right bucket with the desired phase. The primary technique for accomplishing this phase alignment is to reset the DR RF NCO in synch with the bucket zero marker in the recycler (RRAA) and to provide the beam extraction pulse also aligned with the RRAA marker. The kicker requires many turns of the Recycler to charge and the AC dipole for extinction of excess protons also has a long settling time

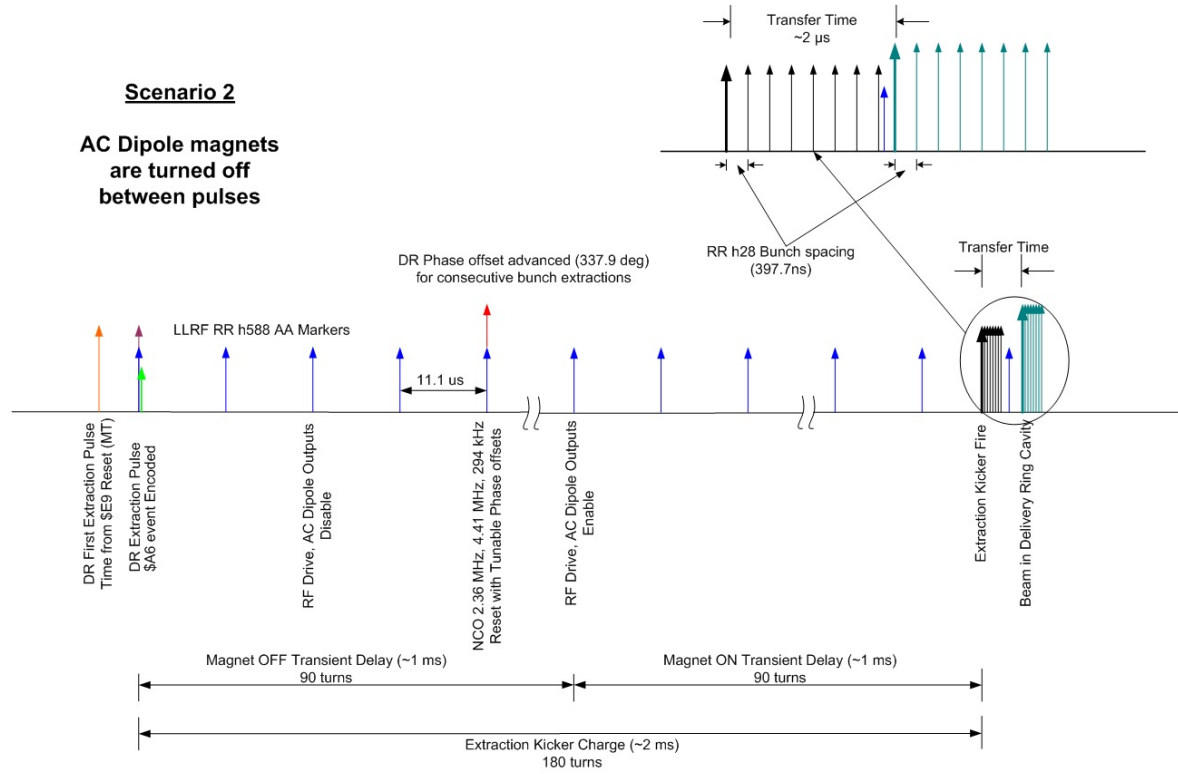


Figure 7: Beam transfer timing with phase alignment

of over 600 μ s. In order to provide adequate time for these purposes, the beam extraction signal is provided about 2 ms or a 180 turns (11.1 μ s each) prior to the kicker firing. This delay plus the transit time of about 2 μ s for the 2000ft distance, the beam has to travel, will allow the beam to land in the desired bucket with the proper injection phase. For the DR RF cavity, the drive is turned off prior to the NCO

reset. One turn after the NCO reset, the RF drive is turned on again. The DR RF cavity has a rise time of 7.5 μ s which is less than 1 turn. At the time of resetting and restarting the NCO in the FPGA, a specific phase offset can be provided to the output. For successive bunches, the bunch spacing of 397.7 ns of the 2.5 MHz can be accounted for with a corresponding phase offset of 337.9 degrees. This offset input can also be used for tuning the injection phase.

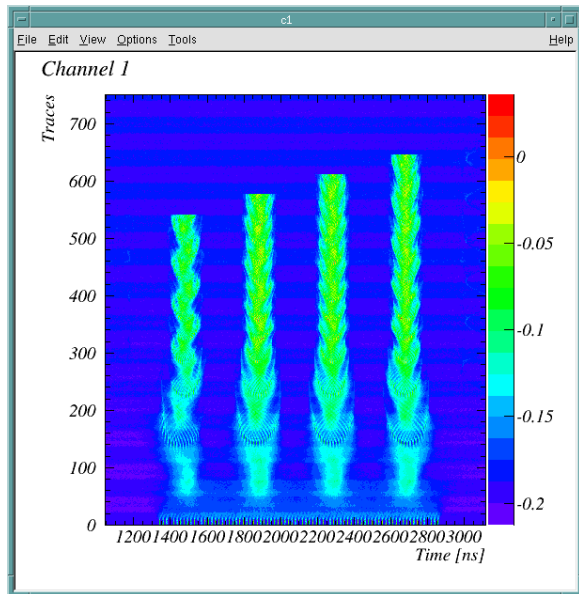


Figure 8: Coalescing of 2.5 MHz bunches

RESULTS AND CONCLUSION

The beam coalescing results from initial beam commissioning tests are shown in Fig. 8. One batch of 84, 53 MHz bunches are coalesced into 4, 2.5 MHz bunches before extraction to the muon $g - 2$ target. The machine cycle to cycle jitter in the 2.5 MHz phase wrt the 53 MHz bucket zero marker was measured to be less than 1 ns. The beam quality requirements for Muon $g - 2$ which are more stringent than the Mu2e experiment, were achieved in the initial beam measurements.

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